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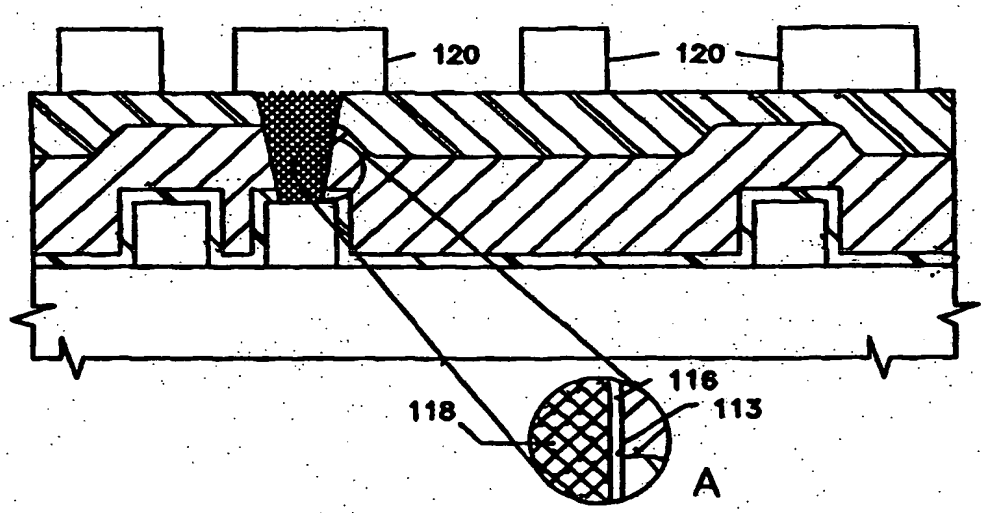
(54) Title: A FLUORINATED OXIDE LOW PERMITTIVITY DIELECTRIC STACK FOR REDUCED CAPACITIVE COUPLING



(57) Abstract

A low permittivity interlevel structure comprising a dielectric formed on the topography of a semiconductor substrate. The dielectric comprises a lower region proximal to the semiconductor substrate, an intermediate region comprised of an oxide into which fluorine is incorporated in an atomic concentration of approximately four to ten percent, and an upper region. A method of forming the dielectric structure includes forming a first interconnect level on a substrate. A first dielectric layer, preferably a CVD oxide, is formed on the topography defined by the first interconnect and the substrate. A second dielectric layer, having a dielectric constant lower than the first dielectric layer, is then formed on the first dielectric layer. A third dielectric layer is formed on the second dielectric layer. The second dielectric layer is preferably formed in a CVD chamber from a silane or TEOS source and a fluorinating material such as SiF_4.

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A FLUORINATED OXIDE LOW PERMITTIVITY DIELECTRIC STACK FOR REDUCED CAPACITIVE COUPLING

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates to semiconductor device fabrication and more particularly to a low permittivity interlevel dielectric structure and method for producing the same.

2. Description of the Relevant Art

An integrated circuit includes numerous conductors extending across the topography of a monolithic substrate. A set of interconnect lines (or conductors) which serve to electrically connect two or more components within a system is generally referred to as a "bus". A collection of voltage levels are forwarded across the conductors to allow proper operation of the components. For example, a microprocessor is connected to memories and input/output devices by certain bus structures. There are numerous types of busses which are classified according to their operation. Examples of well-known types of busses include address busses, data busses, and control busses.

Conductors within a bus generally extend parallel to each other across the semiconductor topography. The conductors are isolated from each other and from underlying conductive elements by a dielectric, a suitable dielectric being, for example, silicon dioxide ("oxide"). Conductors are thereby lithography patterned across the semiconductor topography, wherein the topography comprises a substrate with a dielectric placed thereon. The topography can also include one or more layers of conductors which are sealed by an upper layer of dielectric material. Accordingly, the layers of conductors overlaid with a dielectric present a topography upon which a subsequent layer of conductors can be patterned.

Conductors are made from an electrically conductive material, a suitable material includes Al, Ti, Ta, W, Mo, polysilicon, or a combination thereof. Substrate includes any type of material which can retain dopant ions and the isolated conductivity regions brought about by those ions. Typically, substrate is a silicon-based material which receives p-type or n-type ions.

Generally speaking, interconnect lines (or conductors) are fashioned upon the topography and spaced above an underlying conductor or substrate by a dielectric of thickness T_{di}. Each conductor is dielectrically spaced from other conductors within the same level of conductors by a distance T_{di}. Accordingly, interlevel capacitance C_{LS} (i.e., capacitance between conductors on different levels) is determined as follows:

$$C_{LS} \approx \varepsilon W_L L / T_{di} \qquad \text{(Eq. 1)}$$

Further, the intralevel capacitance C_{LL} (i.e., capacitance between conductors on the same level) is determined as follows:

$$C_{LL} \approx \varepsilon T_c L/T_{d2} \qquad \text{(Eq. 2)}$$

. where ε is the permittivity of the dielectric material (the dielectric material between the conductor and substrate or the dielectric material between conductors). W_L is the conductor width. T_c is the conductor thickness, and L is the conductor length. Resistance of the conductor is calculated as follows:

$$R = (\rho L)/W_L T_c \qquad \text{(Eq. 3)}$$

. where ρ represents resistivity of the conductive material, and T_c is the interconnect thickness. Combinations of equations 1 and 3, and/or equations 2 and 3 indicate the propagation delay of a conductor as follows:

$$RC_{LS} \approx \rho\varepsilon L^2/T_c T_{d1} \qquad \text{(Eq. 4)}$$

$$RC_{LL} \approx \rho\varepsilon L^2 W_L T_{d2} \qquad \text{(Eq. 4)}$$

Propagation delay is an important characteristic of an integrated circuit since it limits the speed (frequency) at which the circuit or circuits can operate. The shorter the propagation delay, the higher the speed of the circuit or circuits. It is therefore important that propagation delay be minimized as much as possible within the geometric constraints of the semiconductor topography.

Equation 4 shows that the propagation delay of a circuit is proportional to the parasitic capacitance values (C_{LL}) between laterally spaced conductors, and parasitic capacitance values (C_{LS}) between vertically spaced conductors or between a conductor and the underlying substrate. As circuit density increases, lateral spacing and vertical spacing between conductors decrease and capacitance C_{LL} increases. Meanwhile, planarization mandates to some extent a decrease in vertical spacing. Shallow trench processing, recessed LOCOS processing, and multi-layered interlevel dielectrics can bring about an overall reduction in vertical spacing and therefore an increase in C_{LS}. Depending upon the geometries associated with a particular device, either C_{LL} or C_{LS} can reduce the performance of the device. Integrated circuits which employ narrow interconnect spacings thereby define C_{LL} as a predominant capacitance, and integrated circuits which employ thin interlevel dielectrics define C_{LS} as a predominant capacitance.

It is therefore important to minimize propagation delay especially in critical speed paths. Given the constraints of chemical compositions, it is not readily plausible to reduce the resistivity ρ of conductor materials. Geometric constraints make it difficult to increase conductor thickness T_c or dielectric thickness T_{d1} or T_{d2}. Still further, instead of reducing length L of a conductor, most modern integrated circuits employ long interconnect lines which compound the propagation delay problems. Accordingly, a need arises for instituting a reduction in propagation delay but within the chemical and geometric constraints of existing fabrication processes. It is therefore desirable that a fabrication process be derived which can reduce propagation by reducing the permittivity ε of dielectric material. More specifically, the desired process must be one which reduces permittivity of dielectric

material arranged between horizontally displaced or vertically displaced conductors. As such, it would be desirable to employ a fabrication technique in which dielectrics between conductors achieve low permittivity.

SUMMARY OF THE INVENTION

The problems outlined above are in large part addressed by a dielectric fabrication process that produces a low permittivity dielectric between the interconnect lines arranged within the same elevation level ("intralevel permittivity") and between interconnect lines within two separate planes or levels ("interlevel permittivity"). A patterned layer of conductive material which forms a first interconnect level is formed on a semiconductor substrate. Next, a first dielectric is formed on the substrate and the first interconnect level. The first dielectric preferably comprises SiO_2 formed from a silane or TEOS source in a plasma enhanced chemical vapor deposition chamber at approximately 375° C. In one embodiment, the first dielectric layer is 100 to 1000 angstroms thick.

A second dielectric layer is then formed upon the first dielectric layer. The permittivity of the second dielectric is lower than the permittivity of the first dielectric. The second dielectric layer is preferably comprised of a CVD oxide into which fluorine is incorporated. The atomic percentage of fluorine incorporated into the second dielectric layer in one embodiment is between 4% and 10% and the thickness of the second dielectric layer is preferably greater than 1000 angstroms.

A third dielectric, preferably a non-fluorinated CVD oxide formed from a silane or TEOS source, is then formed upon the second dielectric to provide a thermodynamically stable capping layer for the second dielectric layer. In one embodiment, the third dielectric is preferably between 500 to 3500 angstroms in thickness. Formation of the third dielectric layer can be followed by a planarization step preferably achieved with a chemical mechanical polish.

The dielectric "stack" (comprised of the first, second, and third dielectric layers) has a dielectric constant that is preferably less than 3.5 (compared to conventional CVD oxides which have dielectric constants in the range of 3.8 to 4.5). In one embodiment of the process, the dielectric stack is formed in a single deposition step with the fluorine being incorporated *in situ* during an intermediate portion of the deposition cycle. The third dielectric layer is provided because it is believed that fluorinated oxides may become unstable in air when the percentage of fluorine incorporated into the film exceeds approximately six to eight percent.

Broadly speaking, the present invention contemplates an interlevel dielectric comprising a first dielectric layer formed on a topography cooperatively defined by a semiconductor substrate and a patterned first interconnect level formed on the semiconductor substrate. Preferably, the first dielectric layer comprises CVD oxide formed from a silane or TEOS source. A second dielectric layer, having a dielectric constant less than the dielectric constant of the first dielectric layer, is formed on the first dielectric layer. In an exemplary embodiment, the lower permittivity of the second dielectric layer is achieved by incorporating fluorine into a CVD oxide in an atomic

concentration of approximately four to ten percent. A third dielectric layer is formed on the second dielectric layer.

The present invention further contemplates a method of forming an interlevel dielectric on a substantially planar first set of interconnects that is formed on an upper surface of a semiconductor substrate. A first dielectric layer, preferably a CVD oxide, is formed on the topography defined by the first set of interconnects and the semiconductor substrate. A second dielectric layer is then formed on the first dielectric layer. The dielectric constant of the second dielectric layer is lower than the dielectric constant of the first dielectric layer. The second dielectric layer is preferably an oxide deposited in a CVD chamber using a TEOS or silane source coupled with a fluorinating material to produce an oxide layer having an atomic concentration of fluorine of approximately four to ten percent. A third dielectric is then formed on the second dielectric layer.

The present invention still further contemplates a method of forming a interlevel dielectric comprising forming a lower, intermediate, and upper sections in a single CVD process wherein a fluorinating material, such as SiF_4, is introduced into the chamber during an intermediate stage of the deposition.

The present invention still further contemplates an interlevel dielectric comprising an oxide formed on a topography cooperatively defined by a semiconductor substrate and a first level interconnect, wherein the oxide comprises lower, intermediate, and upper regions, the intermediate region containing an approximately four to ten percent atomic concentration of fluorine.

BRIEF DESCRIPTION OF THE DRAWINGS

Other objects and advantages of the invention will become apparent upon reading the following detailed description and upon reference to the accompanying drawings in which:

Fig. 1 is a partial cross-sectional view of a semiconductor substrate upon which a first level of interconnects and an oxide layer have been formed;

Fig. 2 is a processing step subsequent to that shown in Fig. 1 in which a second dielectric layer has been formed on the first dielectric layer, the second layer having a lower permittivity than the first dielectric;

Fig. 3 is a processing step subsequent to that shown in Fig. 2 in which a third dielectric has been formed on the second dielectric;

Fig. 4 is a processing step subsequent to that shown in Fig. 3 in which an upper surface of the third dielectric has been planarized to produce a substantially planar upper surface;

Fig. 5 is a processing step subsequent to that shown in Fig. 4 in which a contact has been formed through the third, second, and first dielectrics to the first interconnect level; and

Fig. 6 is a processing step subsequent to that shown in Fig. 5 in which the contact has been filled with a conductive material and a second level of interconnect has been formed on the third dielectric.

While the invention is susceptible to various modifications and alternative forms, specific embodiments thereof are shown by way of example in the drawings and will herein be described in detail. It should be understood, however, that the drawings and detailed description thereto are not intended to limit the invention to the particular form disclosed, but on the contrary, the intention is to cover all modifications, equivalents and alternatives falling within the spirit and scope of the present invention as defined by the appended claims.

DETAILED DESCRIPTION OF THE DRAWINGS

Fig. 1 shows semiconductor substrate 100, a first interconnect level 102, and first dielectric 104. Substrate 100 is typically comprised of a single crystal silicon wafer into which transistors and isolation regions are formed through a series of processing steps well known in the art. An upper surface of substance 100 may include a dielectric for isolating first interconnect level 102 from the underlying transistor regions. This dielectric typically has a plurality of contact openings for selectively coupling first interconnect level 102 to the transistor regions. First level interconnect 102 comprises a plurality of interconnect lines that connect the underlying transistors in a specified manner. First interconnect level 102 is typically formed through a physical vapor deposition step using an aluminum target. After first interconnect level 102 is deposited, photoresist is deposited on the first interconnect level 102 and patterned in a photolithography step. Individual interconnect lines are then formed in an etch step. After formation of first interconnect level 102, a first dielectric 104 is formed upon the topography cooperatively defined by substrate 100 and first interconnect level 102. Formation of first dielectric 104 is preferably carried out by depositing CVD oxide formed from a TEOS or a silane source.

Fig. 2 shows a processing step subsequent to that shown in Fig. 1 in which a second dielectric 106 has been formed on first dielectric 104. Second dielectric 106 has a dielectric constant K_2 which is less than the dielectric constant K_1 of first dielectric 104. In one embodiment, first dielectric 104 is approximately 100 - 1000 angstroms in thickness, while second dielectric 106 is approximately 3,000 - 10,000 angstroms thick. Like first dielectric 104, second dielectric 106 is preferably formed in a CVD chamber with a TEOS or a silane source. To achieve a lower permittivity film however, one embodiment incorporates a fluorinating material into the CVD chamber during formation of second dielectric 106. The fluorinating material can be SiF_4, CF_4, or C_2F_6 in various embodiments. Incorporating fluorine into second dielectric 106 is believed to result in a lower permittivity dielectric. Formation of second dielectric 106 is controlled such that the atomic concentration of fluorine in second dielectric 106 is preferably between 4% and 10%. While incorporating higher percentages of fluorine into second dielectric 106 is believed to result in a lower permittivity film, it is also believed that the fluorinated oxide may become thermodynamically unstable at fluorine concentrations greater than approximately 6-8%. Accordingly, a first embodiment of second dielectric 106 has a low concentration of fluorine, low concentration being defined as less than 6%. The low concentration embodiment might have the advantage of not requiring a third dielectric formed on top of the fluorinated film as discussed below. In a high concentration embodiment (where high

concentration is defined as greater than 6%), second dielectric 106 may require formation of a passivating film on top as disclosed below.

Fig. 3 shows a processing step subsequent to Fig. 2 in which third dielectric 108 has been formed on second dielectric 106. Third dielectric 108 is preferably formed in a CVD chamber with a TEOS or silane source, wherein the chamber has been purged of fluorinating material. Third dielectric 108 has an upper surface 110 which may be planarized using a chemical mechanical polish or a resist etchback process to achieve a substantially planar upper surface 110 as shown in Fig. 4. It is believed that third dielectric 108 provides a thermodynamically stable capping layer for fluorinated oxide 106. In embodiments in which fluorinated film 106 has a concentration of fluorine below six percent, third dielectric 108 may be optionally eliminated.

First dielectric 104, second dielectric 106 and third dielectric 108 can be formed in a single CVD deposition process in which a fluorinating material is introduced into the CVD chamber during an intermediate stage of the deposition. In this embodiment, interlevel dielectric 107 is formed comprising lower region 107a, intermediate region 107b, and upper region 107c, wherein intermediate region 107b has a fluorine concentration of approximately 4% to 10%.

Turning now to Fig. 5, a processing step subsequent to that of Fig. 4 is shown in which contact via 112 has been etched into third dielectric 108, second dielectric 106, and first dielectric 104 to first interconnect level 102. The formation of contact via 112 is preferably accomplished with a plasma etch process. Formation of contact via 112 exposes region 114 of second dielectric 106. In those embodiments in which a second dielectric 106 has a high concentration of fluorine, it may be undesirable to expose regions 114 since second dielectric 106 may be thermodynamically unstable. Accordingly, a passivating film 116, as shown in Fig. 6, can be formed on the sidewall 113 of contact via 112. Passivating film 116 can be comprised of SiO_2 formed in a CVD chamber void of fluorinating material. After formation of contact via 112 and the optional formation of passivating layer 116, contact via 112 is filled with a conductive material 118. Conductive material 118 is commonly formed in a CVD process with a tungsten source. After deposition of conductive material 118, a mechanical polish can be performed to remove conductive material 118 from regions exterior to contact via 112. Subsequently, a second interconnect level can be formed, preferably from a PVD aluminum, and patterned as shown in Fig. 6.

As would be obvious to one skilled in the art having the benefit of this disclosure, the present invention discloses a novel and useful method of incorporating a low permittivity dielectric into an interlevel structure of a semiconductor device. The embodiments shown are merely exemplary of a single form of numerous forms. Various modifications and changes may be made to the configurations shown as would be obvious to a person skilled in the art having the benefit of this disclosure. It is intended that the following claims be interpreted to embrace all such modifications and changes and, accordingly, the specification and drawings are to be regarded in an illustrative rather than a restrictive sense.

WHAT IS CLAIMED IS:

1. An interlevel dielectric comprising:

a first interconnect level formed and patterned on a semiconductor substrate, said first interconnect level and said substrate cooperatively defining a topography;

a first dielectric layer formed on said topography;

a second dielectric layer formed on said first dielectric layer and having a dielectric constant less than a dielectric constant of said first dielectric layer wherein said second dielectric layer comprises an oxide having an atomic concentration of fluorine between 4 and 10 percent; and

a third dielectric layer formed on said second dielectric.

2. The dielectric of claim 1 wherein said first and third dielectric layers comprise oxide.

3. The dielectric of claim 1 wherein said dielectric stack contains one or more contact via, each said one or more contact via having a substantially cylindrical sidewall extending from an upper surface of said third dielectric to said first interconnect level.

4. The dielectric of claim 3 further comprising a passivating film on said substantially cylindrical sidewall of each said one or more contact via.

5. The dielectric of claim 4 wherein said passivating film comprises an oxide.

6. The interlevel dielectric of claim 1 wherein said interlevel dielectric has a composite dielectric constant less than 3.5.

7. A method of forming an interlevel dielectric, comprising the steps of:

forming a substantially planar first set of interconnects on an upper surface of a semiconductor substrate, said first set of interconnects and said upper surface of said substrate cooperatively define a topography;

forming a first dielectric layer on and substantially conformal to said topography,

forming a second dielectric layer having a dielectric constant less than or equal to a dielectric constant of said first dielectric layer on said first dielectric layer by depositing an oxide having an atomic concentration of fluorine of approximately 4 to 10 percent on said first dielectric layer; and

forming a third dielectric layer on said second dielectric layer, whereby said first, second, and third dielectric layers cooperatively define a dielectric stack.

8. The method of claim 7 wherein the step of forming said first and third dielectric layers comprises depositing an oxide in a chemical vapor deposition chamber using a TEOS or silane source.

9. The method of claim 7 wherein said depositing of said second dielectric is accomplished in a chemical vapor deposition chamber using a TEOS or silane source gas into which fluorine is incorporated.

10. The method of claim 7 wherein the steps of forming said first, second, and third dielectric layers are achieved in a single chemical vapor deposition cycle using a TEOS or silane source.

11. The method of claim 10 wherein said single chemical vapor deposition cycle comprises an initial stage, an intermediate stage during which a fluorinating material is introduced into said chamber, and a latter stage prior to which said fluorinating material is purged from said chamber.

12. The method of claim 7 further comprising the step of plasma etching one or more contact vias into said first, second, and third dielectric layers to said first interconnect level wherein each said one or more contact vias has a substantially cylindrical sidewall.

13. The method of claim 12 further comprising forming a passivating film on each said one or more substantially cylindrical sidewalls.

14. The method of claim 13 wherein the step of forming said passivating film comprises depositing an oxide on each said one or more substantially cylindrical sidewalls.

15. The method of claim 7 wherein said interlevel dielectric has a composite dielectric constant less than 3.5.

16. An interlevel dielectric formed by the process of claim 7.

17. An interlevel dielectric comprising:

an oxide formed on a topography cooperatively defined by a semiconductor substrate and a first level interconnect formed and patterned on said substrate, wherein said oxide comprises a lower region, an intermediate region, and an upper region and wherein said intermediate region of said oxide has a atomic concentration of fluorine of approximately four to ten percent.

18. The interlevel dielectric of claim 17 wherein said intermediate region of said oxide is formed in a chemical vapor deposition chamber into which a fluorinating material is introduced.

19. The interlevel dielectric of claim 18 wherein said fluorinating material comprises SiF_4.

FIG. 1

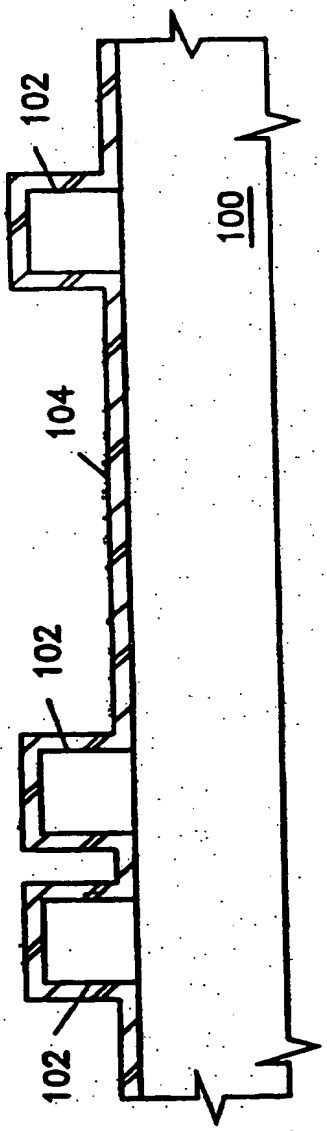


FIG. 2

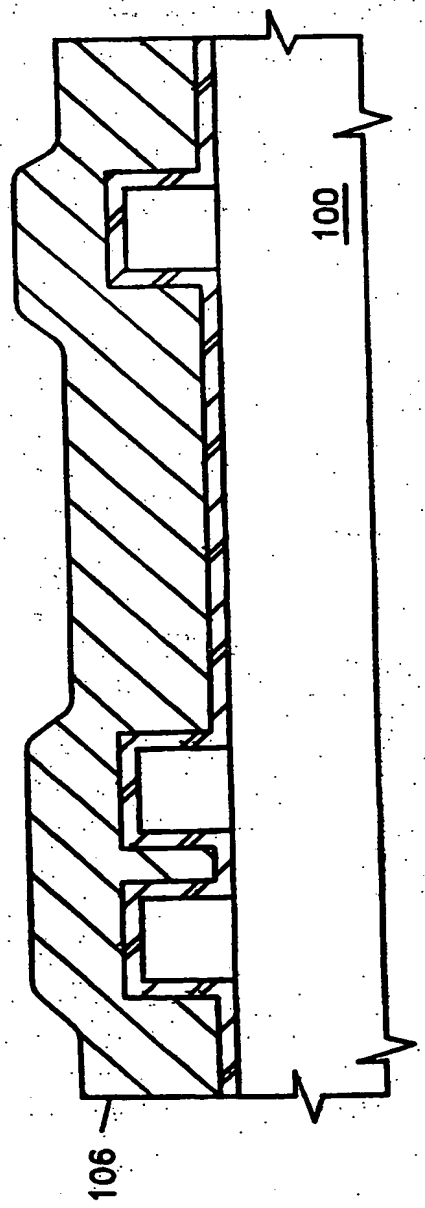


FIG. 3

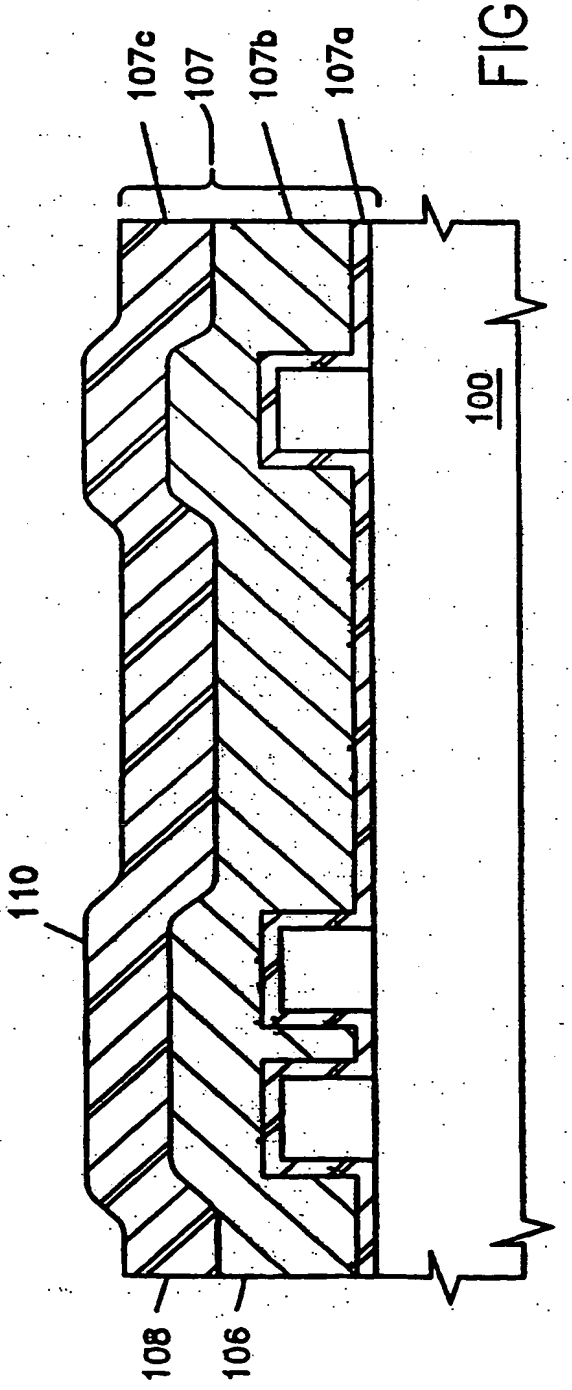


FIG. 4

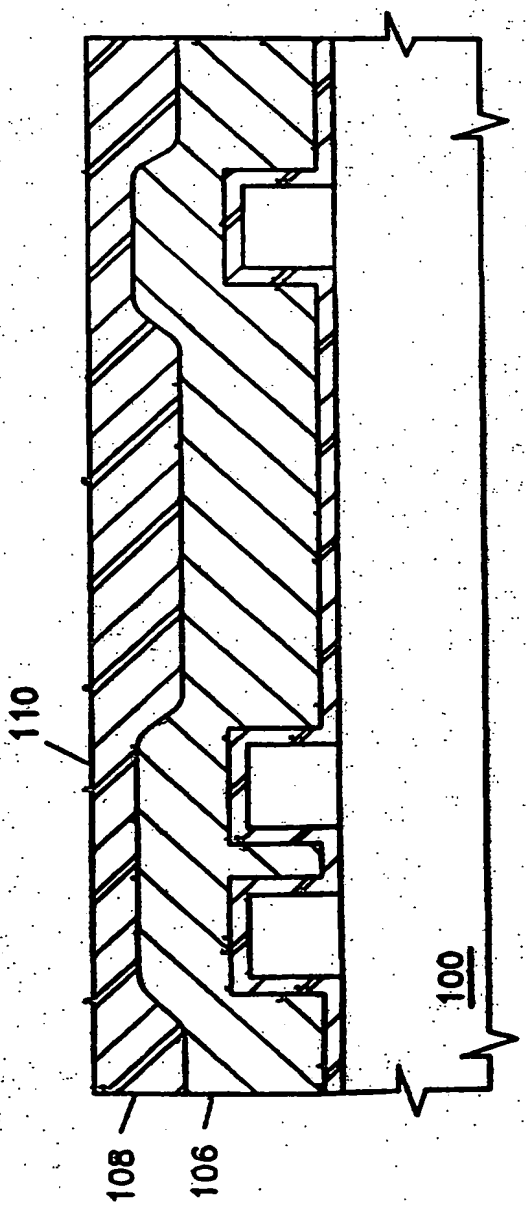


FIG. 5

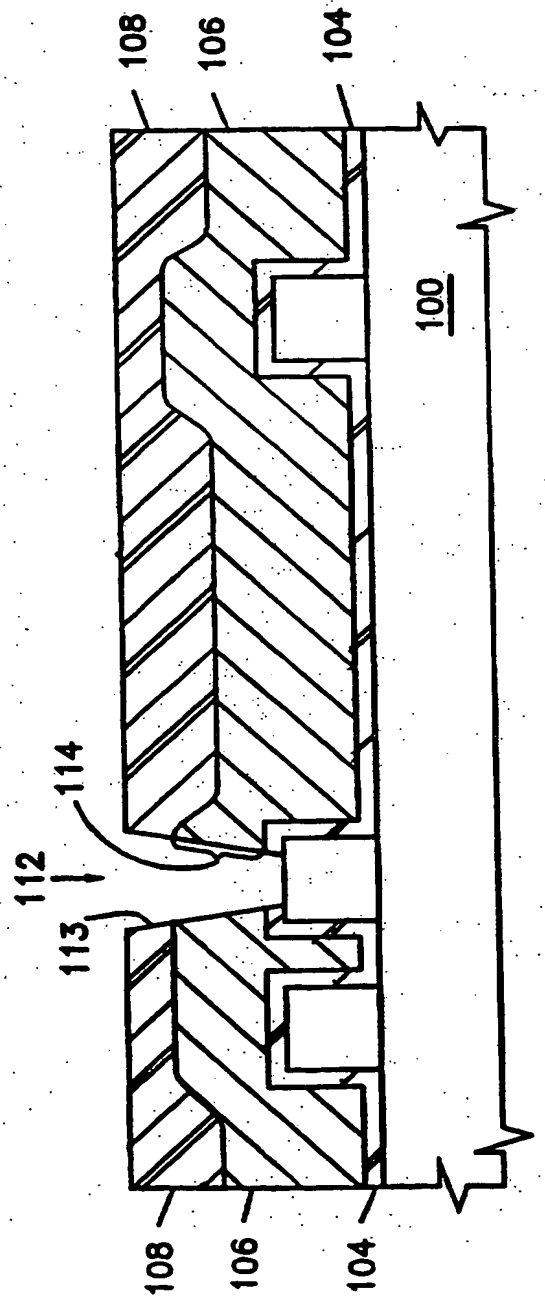
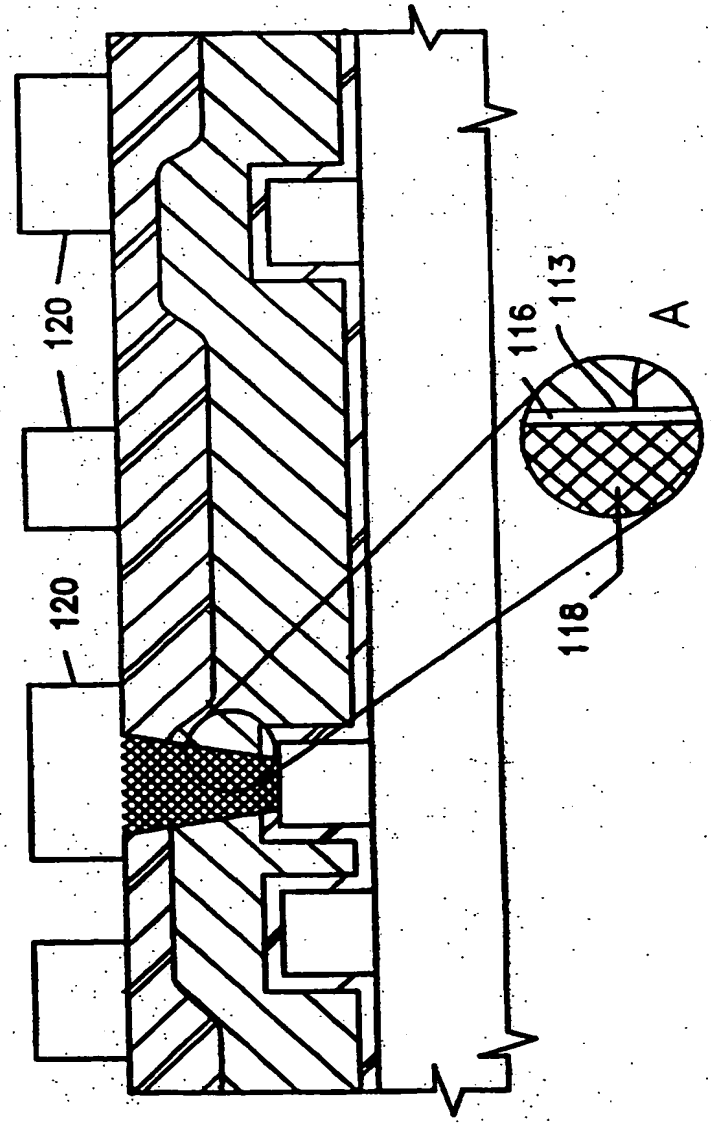


FIG. 6



INTERNATIONAL SEARCH REPORT

Int. ional Application No
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A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H01L21/316 H01L23/532 C23C16/40

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 H01L C23C

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

	Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
6	X	EP 0 706 216 A (SONY CORP) 10 April 1996 see page 1, line 7 - line 8 see page 1, line 49 - page 2, line 5 see page 4, line 6 - line 36	1-9, 12-18
	Y	---	10,11,19
6	X	US 5 334 552 A (HOMMA TETSUYA) 2 August 1994 see column 1, line 54 - column 2, line 30 see column 5, line 19 - column 6, line 47	1,7,16, 17
6	Y	---	10,11,19
		US 5 429 995 A (NISHIYAMA YUKIO ET AL) 4 July 1995 see column 1, line 38 - line 42 see column 10, line 38 - line 40 see figure 27	

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[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

* Special categories of cited documents :

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1 Date of the actual completion of the international search
27 March 1997

Date of mailing of the international search report
28.04.97

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Authorized officer
Machek, J

Form PCT/ISA/210 (second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

Int onal Application No
PCT/US 96/20485

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
T	SYMPOSIUM ON VLSI TECHNOLOGY. DIGEST OF TECHNICAL PAPERS, HONOLULU, JUNE 7 - 9, 1994, no. SYMP. 14, 7 June 1994, INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS, page 59/60 XP000498582 IDA J ET AL: "REDUCTION OF WIRING CAPACITANCE WITH NEW LOW DIELECTRIC SIOF INTERLAYER FILM FOR HIGH SPEED/LOW POWER SUB-HALF MICRON CMOS" see the whole document see figure 1 -----	1,7,17

Form PCT/ISA/210 (continuation of second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

Information on patent family members

Inter onal Application No
PCT/US 96/20485

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US 5429995 A	04-07-95	JP 7074245 A	17-03-95

FIG. 1

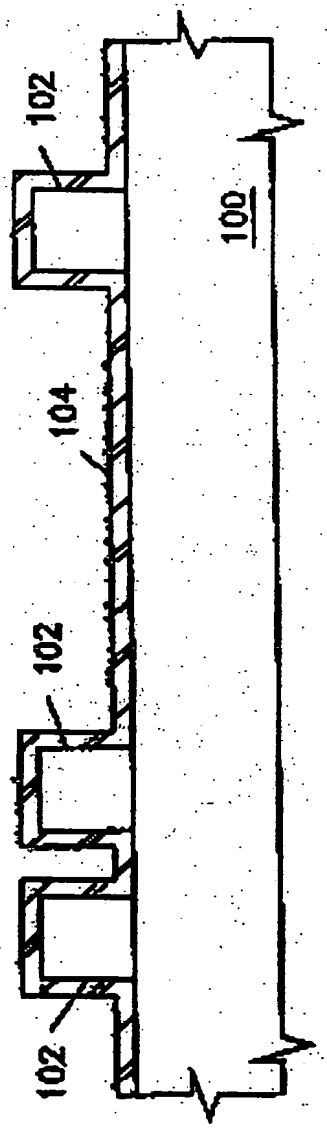

FIG. 2

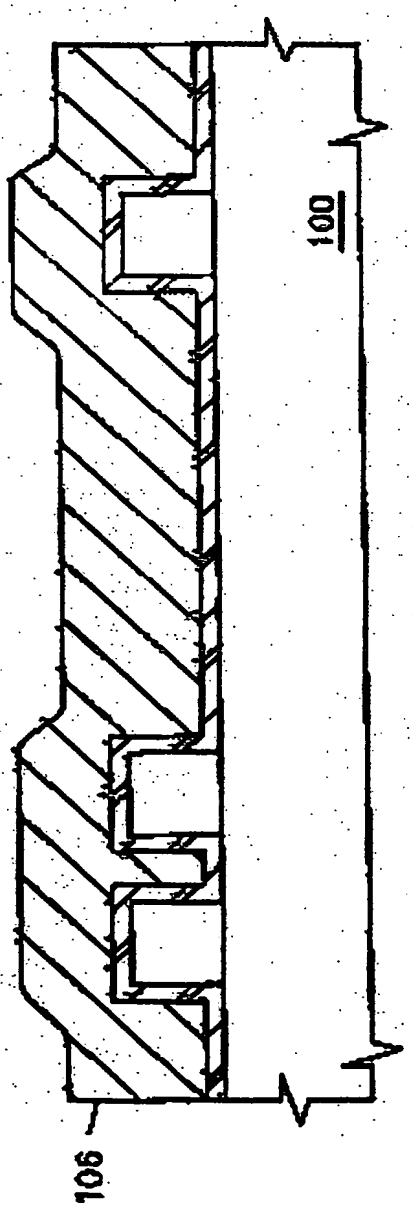

FIG. 3

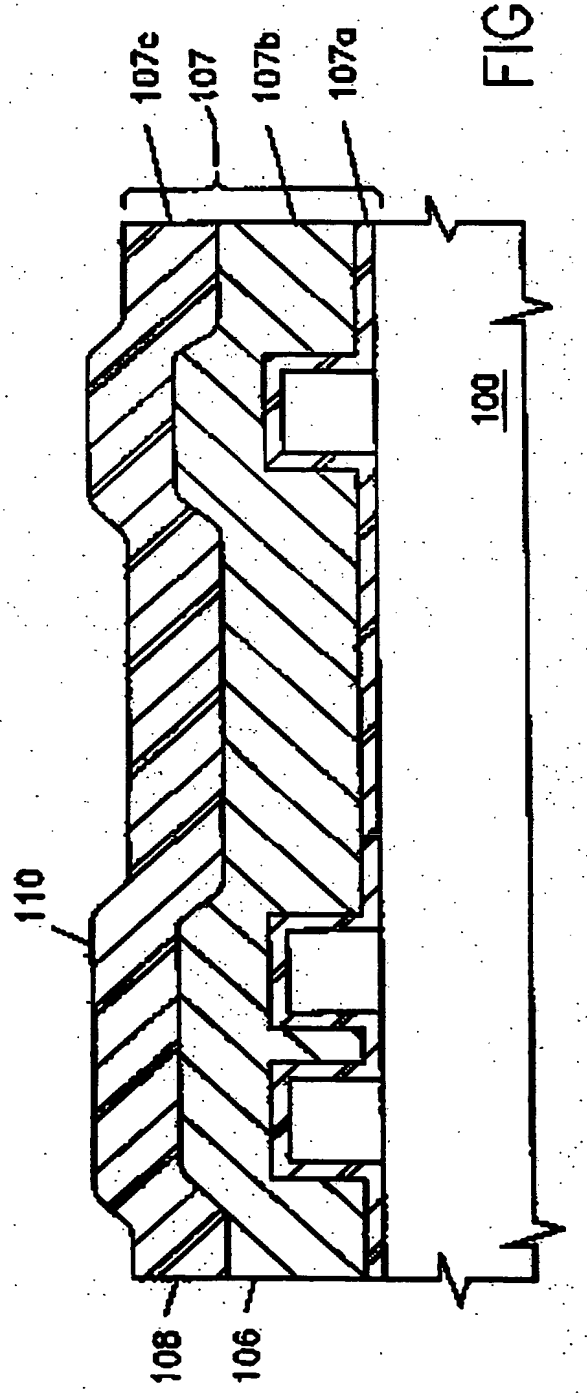

FIG. 4

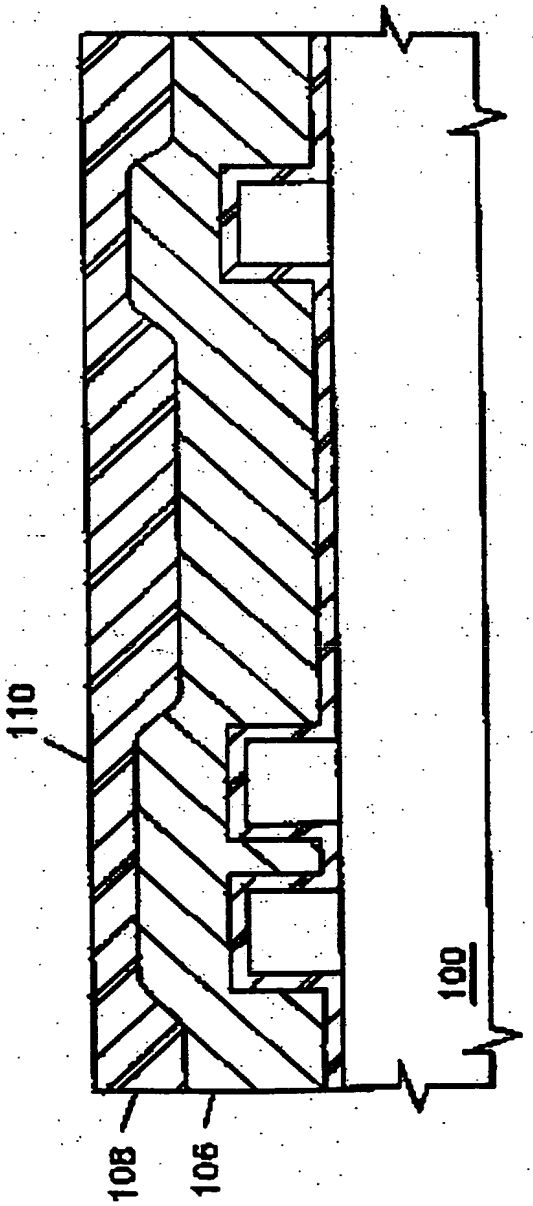

FIG. 5

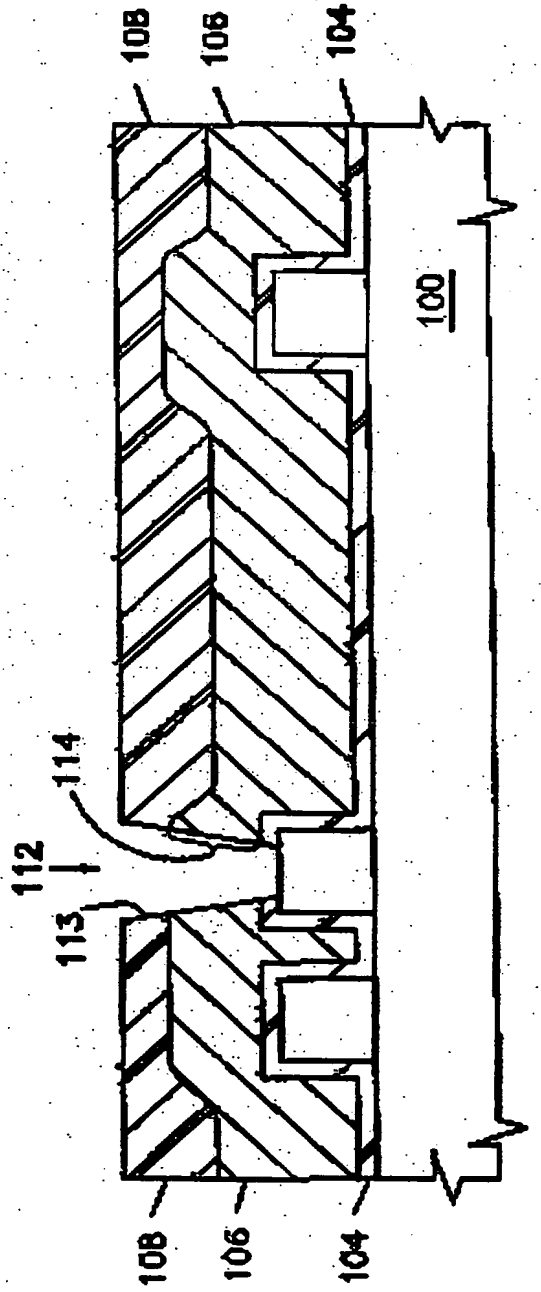

FIG. 6